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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
CRAIG, DWIN M	

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 12/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/815,446	BODE ET AL.	
	Examiner	Art Unit	
	Dwin M. Craig	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-34 have been presented for reconsideration based on Applicants' arguments.

Response to Arguments

2. Applicants' arguments presented in the 9/2/2005 response have been fully considered.

The Examiner's response is as follows.

2.1 On page 13 of the 9/2/2005 responses Applicants' argued,

For example,

[The Examiner considers "level-to-level metrology" in Ausschnitt to be equivalent as wafer-mean error metrology analysis of the present invention. Other misapplications were also made in the Office Action, as described below. Ausschnitt merely discloses performing analysis of within level overlay errors as well as of level-to-level field overlay errors. The level-to-level disclosure in Ausschnitt merely refers to multiple layers of the wafers, such as the "level A" 66 and the "level B" 60. See Figure 8, column 3, lines 44-49. Ausschnitt also refers to the fact that it is directed to the absolute error relating to level A and level B and not necessarily to the relative error between level A and level B. See column 3, lines 49-52. Applicants respectfully assert that the Examiner misunderstands the level-to-level error disclosed by Ausschnitt. Ausschnitt is clear as to the fact that the level-level term relates to level-to-level field overlay error and not to wafer-mean error called for by the claims of the present invention.]

The Examiner respectfully notes the following, Applicants' specification and claims fails to disclose a definition of *"wafer-mean error"* such that this definition reads differently than the disclosed teachings of the *Ausschnitt et al.* reference. The Examiner carefully reviewed Applicants' specification and drawings and notes that Applicants' specification clearly defines *"field-to-field"* error in silicon wafer production and also provides a specific definition of *"wafer-mean error"* see page 14 of the specification, where the following is discussed, *"A wafer-mean error data set relates to the average overlay error for a particular wafer as a whole from one process to the other"*. The Examiner notes that the *Ausschnitt et al.* reference discloses the exact same process as argued and disclosed in Applicants' specification and arguments, that

the *"wafer-mean error"* is the same as the, *"translational alignment errors at all levels is applied"*, as disclosed in the Examiner's applied prior art rejection.

2.2 The Examiner respectfully notes that the rest of Applicants' unpersuasive arguments, as provided in the 9/2/2005 responses, as well as the lack of amendment to Applicants' expressly claimed limitations, have failed to overcome the prior art rejection in view of the *Ausschnitt et al.* reference.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-34 are rejected under 35 USC § 102(b) as being anticipated by **US Patent 5,877,861 Ausschnitt et al.**

3.1 As regards Independent Claims 1, 11, 15, 16, 26 and 29 and using independent Claim 1 as an example, the *Ausschnitt et al.* reference discloses,

processing at least one semiconductor device (Figure 12 item 80 EXPOSED WAFER),

acquiring metrology data from said processed semiconductor device; (Abstract),

performing a field-to-field metrology analysis based upon said metrology data to determine a field-mean error; (Col. 2 line 40, The field term alignment errors are calculated from the within-level between-field overlay measurement using the processor. The Examiner notes that field term alignment errors are the same as field-mean error.),

determining a wafer-mean error; (ABSTRACT, Simultaneous use of between-field overlay metrology to control field term alignment error at al levels and *level-to-level* metrology to control file term, and translational alignment errors at all levels is applied. The Examiner notes that Level-to-level metrology is the same as wafer-mean error metrology analysis.),

comparing said field-mean error to said wafer-mean error; (Col. 2 line 42, The correction factors are calculated from the field term alignment errors and the level-to-level overlay measurements using the processor.),

performing residual-error analysis based upon said field-to-field analysis and said wafer-mean error, said residual-error analysis comprising determining whether significant residual error exists as a result of comparing said residual error with a predetermined tolerance, said residual-error being based upon said comparison of said wafer-mean error and said field-mean error data; and (Col. 1 line 20, A requirement of the manufacturing process is to keep the alignment error, between levels, below acceptable product *tolerances*. And Col. 6 line 39, The equations are solved using any technique such as "least squares" best fit or any other mathematical technique for solving for the unknown variables based on minimization of the *residual* error.),

performing at least one of a field-level adjustment and a wafer-level adjustment based upon said residual-error analysis. (Col. 2 line 44, the field layers are then aligned based on the correction factors.).

3.2 As regards dependent **Claims 2, 12-14, 17, 28, 32, 33** the *Ausschnitt et al.* reference discloses, processing said semiconductor device in a subsequent manufacturing process based

upon said residual-error analysis (Col. 6 line 42, The calculated terms are fed back to the lithography tool to correct overlay errors...).

3.3 As regards dependent **Claims 3, 18, 27 and 30** the *Ausschnitt et al.* reference discloses wafers (Figure 12 item 80).

3.4 As regards dependent **Claims 4, 19 and 34** the *Ausschnitt et al.* reference discloses field-to-field metrology data analysis (Col. 2 line 37, Next, the level-to-level field and within-level between-field errors are measured using overlay targets and metrology equipment.).

3.5 As regards dependent **Claims 5-10, 20-25 and 31** are all directed towards determining alignment and overlay errors and programming a machine to compensate for these errors. The *Ausschnitt et al.* reference discloses determining alignment errors (Figures 1A-1E. 2A-2C), field errors (Figures 3A-3B, 4, 5, 6), fixing alignment (Figure 7), and programming a machine to calculate and compensate for these measured errors (Summary of the invention Col. 2 lines 30-48).

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

"Real-Time Reactive Ion Etch Metrology Techniques to Enable *In Situ* response Surface Process Characterization" by Pete Klimecky, Craig Garvin, Cecilia G. Galarza, Brook S. Stutzman, Pramod P. Khargonekar and Fred L. Terry, Jr. discloses teachings as regards the use of metrology data in wafer manufacturing, figures 2-7.

"Predictive process control for sub-0.2 um lithography" by Terrence E. Zavecz and Rene Blanquies, pages 1-12 discloses statistical methods of determining errors in wafer manufacturing.

US Patent 6,372,395 discloses comparing different exposure mask patterns in the manufacturing of semiconductor wafers (Abstract).

US Patent 5,243,195 discloses determining the overlay error between the X and Y axis of a exposure mask using Abbe's condition (Abstract).

US Patent 4,397,543 discloses methods of using registration marks for alignment of exposure masks for exposure fields in semiconductor wafers (Abstract).

US Patent 6,587,744 discloses methods of using a controller and feedback methods, involving metrology tools when modeling the manufacture of semiconductor wafers (Abstract).

US Patent 6,163,366 discloses methods of aligning exposure masks on semiconductor wafers during manufacturing (Abstract).

US Patent 5,438,413 discloses metrology methods for dealing with mis-registration of fields on a silicon wafer during manufacturing (Abstract).

US Patent 5,444,538 discloses correction of overlay errors when manufacturing semi-conductor wafers.

US Patent 6,699,627 discloses recording alignment errors in a database for use during the processing and production of silicon wafers (Abstract, Figure 34, Col. 4 lines 28-49).

US Patent 5,989,761 discloses determining errors due to rotation angles for overlays in semiconductor exposure masks when manufacturing wafers (Abstract, figures 5-10).

US Patent 6,445,206 discloses determining the difference in errors in lots of wafers and using the information by utilizing a database (Figures 1-3 and Col. 9 lines 6-30).

4.1 Claims 1-34 are rejected.

4.2 **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dwin M. Craig whose telephone number is (571) 272-3710. The examiner can normally be reached on 10:00 - 6:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo P. Picard can be reached on (571) 272-3749. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DMC

Paul L. Rodriguez 11/28/05

Primary Examiner
Art Unit 2125